

Amendments to the Claims

1. (CURRENTLY AMENDED) A driver comprising: a first current source (~~I1, amp1~~), an output transistor (~~M1~~), operably coupled to the first current source (~~I1, amp1~~), a mirror transistor (~~M11~~), and a switch (~~SWEN~~) that is configured to selectively couple the mirror transistor (~~M11~~) and the output transistor (~~M1~~) to form a first current mirror (~~M11, M1~~) that controls bias current through the output transistor (~~M1~~).

2. (CURRENTLY AMENDED) The driver of claim 1, wherein the first current source (~~I1, amp1~~) includes a first amplifier (~~amp1~~) that is configured to: compare an output voltage of the output transistor (~~M1~~) to a reference voltage (~~Vref~~), and, provide a driving current to the output transistor (~~M1~~) when the output voltage of the output transistor (~~M1~~) is above the reference voltage (~~Vref~~).

3. (ORIGINAL) The driver of claim 2, wherein the driving current is substantially constant.

4. (CURRENTLY AMENDED) The driver of claim 2, further including a second current source (~~I2, amp2~~) that is configured to provide load current to a load that is coupled to the output transistor (~~M1~~).

5. (CURRENTLY AMENDED) The driver of claim 4, wherein the second current source (~~I2, amp2~~) includes a second amplifier (~~amp2~~) that is configured to provide the load current to the load when the output voltage is substantially equal to the reference voltage (~~Vref~~).

6. (CURRENTLY AMENDED) The driver of claim 5, further including a controller (~~710~~) that is configured to maintain a minimal current to the output transistor (~~M1~~) that prevents the output transistor (~~M1~~) from turning off.

7. (CURRENTLY AMENDED) The driver of claim 4, wherein the second current source (~~I2, amp2~~) is further configured to provide the bias current to the output transistor (~~M1~~).

8. (CURRENTLY AMENDED) The driver of claim 7, further including a compensation circuit (~~M30-32~~) that is configured to control the bias current substantially independent of process variations and temperature.

9. (CURRENTLY AMENDED) The driver of claim 4, wherein the second current source (~~I2, amp2~~) includes a blocking diode (~~D2~~) that isolates the driver from voltages applied to the output transistor (~~M1~~) from sources external to the driver.

10. (CURRENTLY AMENDED) The driver of claim 4, wherein the output transistor (~~M1~~) is of a first channel-type, and the second current source (~~I2, amp2~~) includes a transistor of a second channel-type that differs from the first channel-type.

11. (CURRENTLY AMENDED) The driver of claim 2, wherein the first amplifier (~~amp1~~) is configured to provide configurable gain.

12. (CURRENTLY AMENDED) The driver of claim 1, wherein the first current source (~~I1, amp1~~) includes a second current mirror (~~M2, M3~~) that provides the bias current to an input of the first current mirror (~~M11, M1~~), and a third current mirror (~~M2, M20~~) that provides the bias current to an output of the first current mirror (~~M11, M1~~).

13. (CURRENTLY AMENDED) The driver of claim 1, wherein the mirror transistor (~~M11~~) and the output transistor (~~M1~~) are sized so that the bias current provides a gate-source voltage that is above a threshold voltage of the output transistor (~~M1~~).

14. (CURRENTLY AMENDED) The driver of claim 1, wherein the output transistor (~~M1~~) is configured to have a Miller capacitor (~~Cm~~) coupled between a drain of the output transistor (~~M1~~) and a gate of the output transistor (~~M1~~).

15. (CURRENTLY AMENDED) A driver comprising: a first current source (~~I1, amp1~~); an output transistor (~~M1~~) having a gate operably coupled to the first current source (~~I1, amp1~~), a drain operably coupled to a first node of a bus (~~Vbusp~~), and a source operably coupled to a second node of a bus (~~Vbusn~~); a mirror transistor (~~M11~~) having a gate operably coupled to the gate of the output transistor (~~M1~~), a drain operably coupled to the gate of the output transistor (~~M1~~), and a source; a switch (~~SWEN~~) operably coupled between the source of the mirror transistor (~~M11~~) and the second node of the bus (~~Vbusn~~); and a Miller capacitor (~~Cm~~) coupled between the drain of the output transistor (~~M1~~) and the gate of the output transistor (~~M1~~).

16. (CURRENTLY AMENDED) The driver of claim 15, wherein the first current source (~~I1, amp1~~) includes a first differential amplifier (~~amp1~~) having: a first

input operably coupled to the first node of the bus (~~V_{busp}~~), a second input operably coupled to a reference voltage (~~V_{ref}~~), and an output coupled to the gate of the output transistor (~~M1~~).

17. (CURRENTLY AMENDED) A method of providing a drive current to a bus, comprising: providing a first current to a gate of an output transistor (~~M1~~) during an inactive state, and providing a second current to the output transistor (~~M1~~) in an active state, and providing a third current to the output transistor (~~M1~~) when a voltage (~~V_{BUSP}~~) on the bus reaches a determined voltage, wherein the first current maintains a non-zero voltage at the gate of the output transistor (~~M1~~).